

App. Serial No. 10/534,655
Docket No.: DE 020249 US

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Remarks

Claims 1-7 are currently pending in the patent application. For the reasons and arguments set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The non-final Office Action dated June 27, 2006 indicated two rejections, specifically that: claims 1-7 stand rejected under 35 U.S.C. § 102(b) over Suzuki *et al.* (U.S. 4,291,274); and claims 1-5 stand also rejected under 35 U.S.C. § 102(b) over Tsinker (U.S. 6,323,692).

Applicant has amended the claims to clarify the claim language and to facilitate prosecution. As originally presented, and as presented herein above, the claimed invention is directed to a phase comparator that provides regulating signals responsive to an evaluation of edges of input signals to the phase comparator. In claim 1, the preamble has been amended to provide antecedent basis for the claim term "regulating signals" and to clarify that the regulating signals are reset by each of the reset signals generated by the circuit and each of the additional reset signals generated by the additional circuit.

Applicant respectfully traverses the Section 102(b) rejections of claims 1-7 because the cited portions of the Suzuki reference fail to correspond to all of the claimed limitations. Regarding independent claim 1 (and as relevant to the claims that depend therefrom), the Office Action fails to cite any portion of the Suzuki reference that corresponds to claimed limitations directed to that each of the reset signals and each of the additional reset signals reset the regulating signals.

Moreover, the Suzuki reference fails to teach or suggest claim 1 limitations directed to the additional circuit to evaluate different edges of the first or second input signals and generate additional reset signals therefrom. The Office Action cites flip-flops 10 and 11 of the Suzuki reference as the additional circuit and cites to "R" as the additional reset signals (see, e.g., Fig. 2). However, flip-flops 10 and 11 evaluate the same edges (*i.e.*, the rising edges) of input signals SIG and REF that circuits 8 and 9 evaluate (see, e.g., Fig. 2, Fig. 3 and col. 2, lines 37-60). The Suzuki reference does not teach that at least one additional circuit evaluates different edges of the first or second input signals as in the claimed invention. Moreover, the Office Action cites to "R" of Fig. 2 of the Suzuki reference as both the reset signals and the additional reset signals of the claimed

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invention (see, *e.g.*, page 2, paragraph 3). The Suzuki reference does not teach generating two different sets of reset signals as in the claimed invention. Accordingly, the Section 102(b) rejections of independent claim 1, and claims 2-7 which depend from claim 1, are improper and Applicant requests that they be withdrawn.

Furthermore, regarding claim 7, the cited portions of the Suzuki reference fail to correspond to claimed limitations directed to that the first and second input signals are applied to the additional circuit via an OR gate. The Office Action cites to SIG and REF as the two input signals and cites to flip-flops 27 and 29 as the additional circuit (see, *e.g.*, page 3, last paragraph). However, SIG is applied to the reset of flip-flop 29 and REF is applied to the reset of flip-flop 27; SIG and REF are not applied to the flip-flops via an OR gate as asserted by the Office Action (see, *e.g.*, Figs. 7 and 16). Moreover, the output signals of flip-flops 28 and 30 are applied to flip-flops 27 and 29 via NOR gate 31, not SIG and REF (see, *e.g.*, Figs. 7 and 16). The Suzuki reference does not teach that the input signals are applied to the additional circuit via an OR gate as in the claimed invention.

Applicant traverses the Section 102(b) rejections of claims 1-5 because the cited portions of the Tsinker reference fail to correspond to all of the claimed limitations. Regarding independent claim 1 (and as relevant to the claims that depend therefrom), the Office Action fails to cite any portion of the Tsinker reference that corresponds to claimed limitations directed to that each of the reset signals and each of the additional reset signals reset the regulating signals.

Moreover, the Tsinker reference fails to teach or suggest claim 1 limitations directed to the additional circuit to evaluate different edges of the first or the second input signals and generate additional reset signals therefrom. The Office Action cites flip-flop 202 of the Tsinker reference as the at least one additional circuit and UPDN_RST as the additional reset signal (see, *e.g.*, Fig. 10). However, UPDN_RST is generated by AND gate 210 (see, *e.g.*, col. 20, lines 20-23), not by flip-flop 202 as asserted by the Office Action. Moreover, AND gate 210 is part of the same circuit that generates signals REST_DN and REST_UP which the Office Action cited as the reset signals of claim 1 (see, *e.g.*, Fig. 10). Therefore, the Tsinker reference does not teach that one circuit generates reset signals and that an additional circuit generates additional reset signals as

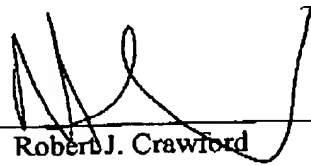
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in the claimed invention. Accordingly, the Section 102(b) rejections of independent claim 1, and claims 2-5 which depend from claim 1, are improper and Applicant requests that they be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of Philips Corporation at (408) 474-9063.

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